

IN THE CLAIMS

Please amend the claims as follows:

① Claims 1-21 (Canceled).

Claim 22 (Currently Amended): The method of manufacturing a semiconductor device according to claim [21] 25, wherein

said each mask pattern of said plural intellectual [properties] property functional circuits has a mark for positioning, and

positioning of said mask patterns is performed by superposing one of said marks on another of said marks such that the intellectual property functional circuits are adjacent to one another and not overlapping.

Claim 23 (Currently Amended): A semiconductor device manufactured by the method according to claim [21] 25.

Claim 24 (Previously Presented): A semiconductor device manufactured by the method according to Claim 22.

Claim 25 (New): A method of manufacturing an electronic circuit having a plurality of separate intellectual property functional circuits on a single semiconductor chip, the method comprising:

storing a library of layout patterns including layout patterns of said intellectual property functional circuits;

storing a diagram of the electronic circuit;

Application Serial No: 09/761,738

Appeal No: 2003-1310

In response to the Official Action dated February 21, 2002  
and the Decision on Appeal and Order mailed February 19, 2004

generating a mask pattern for each of the intellectual property functional circuits  
based on the stored library; and

transferring each of the mask patterns to a predetermined position on the  
semiconductor chip such that the intellectual property functional circuits are adjacent to each  
other and not overlapping.

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